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METHOD AND APPARATUS OF DATA TRANSMISSION

CROSS-REFERENCES TO RELATED APPLICATIONS

The present invention relates to the following U.S. Patent application assigned to the assignee of the present invention. U.S. Serial No. 09/099390,
5 Atushi Miyasita et al. filed on June 18, 1998 entitled "OFDM MODULATOR AND OFDM MODULATION METHOD FOR DIGITAL MODULATED WAVE HAVING GUARD INTERVAL", U.S. Serial No. 09/096454, Seiichi Sano et al. filed on June 11, 1998 entitled "DATA TRANSMISSION APPARATUS AND RECEIVING
10 APPARATUS USING ORTHOGONAL FREQUENCY DIVISION MULTIPLEX MODULATION SYSTEM" and U.S. Serial No. 09/203564, Seiichi Sano et al. filed on December 2, 1998 entitled "SYNCHRONIZATION DETECTION METHOD FOR DATA TRANSMISSION APPARATUS AND DATA TRANSMISSION APPARATUS USING THE
15 SAME" .

BACKGROUND OF THE INVENTION

The present invention relates in general to a method and an apparatus for transmitting data, and more particularly to a method and an apparatus for transmitting data employing an OFDM (Orthogonal Frequency
20 Division Multiplex) system, and a method and an apparatus for receiving an OFDM signal.

In recent years, as for the modulation method which is suitable for being applied to the digital

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audio broadcasting for mobiles and terrestrial digital television broadcasting, the OFDM system which features a robustness to multi path fading and ghost has received much attention. The OFDM system is one of the multi-carrier modulation systems and is a transmission method of subjecting n carriers (n is in the range of several tens to several hundreds) which are orthogonal to one another.

Then, as shown in Fig. 2, the modulated signal is transmitted which is acquired by adding a large number of digital modulated waves to one another and by subjecting the I-axis and the Q-axis to the orthogonal modulation. While as for the above-mentioned digital modulation method, in general, the DQPSK (4 Differential Quadrature Phase Shift Keying) system is often employed, it is also possible to employ the multi-value modulation system such as the 16 QAM (16 Quadrature Amplitude Modulation) or the 32 QAM.

In addition, as shown in Fig. 3, the symbol of the OFDM is constructed such that the guard interval for reducing the influence of the delayed wave is added to the effective data symbol. The guard interval is the signal which is added cyclically to the signal of the effective data symbol. The guard interval is described in, for example, U.S. Serial No. 09/099390 (corresponding to European Patent application No. 98111075.2 filed on June 17, 1998) entitled "OFDM MODULATOR AND OFDM MODULATION METHOD FOR DIGITAL

groups. An example of the constitution of the transmission frame is shown in Fig. 4.

The reception side executes the sync pull-in processing on the basis of the synchronous symbol.

5 Then, the sampling clock frequency on the transmission side is synchronized with the sampling clock frequency on the reception side to demodulate the OFDM signal.

In this connection, a prior art technique relating to sync pull-in based on the synchronous
10 symbol or the like is disclosed in JP-A-7-321762 for example.

SUMMARY OF THE INVENTION

First, description will hereinbelow be given with respect to an example of a configuration of an
15 OFDM digital transmission apparatus to which the present invention is applied and the operation thereof.

Fig. 5 is a block diagram showing a configuration of a transmitter for transmitting therefrom the above-mentioned transmission frame. The configuration
20 and operation of this transmitter will now be described with reference to Figs. 5 and 4, respectively.

As shown in Fig. 4, a first symbol is a null signal synchronous symbol (hereinafter, referred to as "a null symbol" for short, when applicable) and is
25 generated in a null symbol generator 54. The null symbol is zero on I and Q axes with respect to the amplitude thereof, and hence the null symbol is the

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synchronous symbol and the data symbols, and a base band OFDM signal in a frame construction is outputted from a selector 56.

After being inputted to a D/A conversion unit 57 for digital/analog conversion therein, the OFDM signal is up-converted into the signal having an IF (Inter Frequency) band in a base band (BB)/IF conversion unit 58. Then, the OFDM transmission signal is transmitted in transmission frames.

Fig. 6 is a block diagram showing a configuration of a receiver for receiving the above-mentioned OFDM signal.

In the receiver shown in Fig. 6, after the received signal is converted into the signal having the IF band width, the signal having the IF band width is converted into the signal having the frequency band of the base band in an IF/BB conversion unit 61 to acquire the base band OFDM signal. Then, the base band OFDM signal is sampled using the sampling clock from a VCO 67 in an A/D conversion unit 62 to acquire the signal of the reception sample value sequence.

Next, description will hereinbelow be given with respect to the reception side sampling clock recovery processing wherein the sampling clock frequency when carrying out the sampling in the A/D conversion unit 62 is made coincide with the sampling clock frequency of the transmission signal, and a series of processing wherein the transition points of

the frame and the symbol of the reception sample value sequence signal are detected to control the timing of the frame and the symbol period of time in the receiver with reference to Fig. 8.

5 Fig. 8 is a time chart for explaining the operation of a frame counter 68.

The above-mentioned frame timing and symbol timing are counted in reception sampling clocks at an RES terminal of the frame counter 68.

10 First, as a first stage, a null symbol detection unit 63 detects a starting point of the null symbol from the reception sample value sequence signal sent from the A/D conversion unit 62 to output a signal NS exhibiting the rough starting point of the trans-
15 mission frame. The signal NS is inputted to the frame counter 68 and resets the count value of the frame counter 68 at a time TC1.

The frame counter 68 continues to carry out the counting in reception sampling clocks to determine
20 roughly the timing of the current frame and symbol.

In a second stage, since the information relating to the starting point of the frame detected by the null symbol detection unit 63 contains an error, the specific time point on the time base of the trans-
25 mission frame is more accurately detected. For this reason, a time window having a predetermined length is provided on the time base on the basis of the null symbol starting position acquired in the first stage.

tion unit 65 detects the maximum value from the cross-correlation value sequence. The correlation maximum value becomes maximum when the position of the time base coincides with the position of the sweep symbol in the received signal.

Then, the correlation maximum position detection unit 65 operates arithmetically in reception sampling clocks an error on the time base between the position of the time window when outputting the correlation maximum value and a time point of the sweep symbol which is counted on the basis of the null symbol starting position which has been detected in the first stage to output error information ERR.

Since the correlation maximum value position detection unit 65 can detect the sweep symbol position in the reception sample value sequence with high accuracy, the detection unit 65 inputs the error information ERR acquired in the correlation maximum value position detection unit 65 to an LD terminal of the frame counter 68 at a time TC3 to correct the count value. With respect to the correction of the count value, for example, the count value at a time point TC3 is corrected back and forth by the value of the error information ERR, whereby the frame timing of the reception sample value sequence at a starting time point (TC4) of a next frame coincides with the frame timing of the frame counter 68.

In addition, that error information ERR is a

value acquired by counting in reception sampling clocks
an error in time between one frame period of time
counted using the sampling clock on the transmission
side and one frame period of time counted using the
5 reception sampling clock, and is converted into the
frequency error of the received sampling clock.

For this reason, a VCO control unit 66
outputs a signal which is used to control variably the
output clock frequency of a VCO 67 on the basis of the
10 error information ERR from the correlation maximum
value position detection unit 65. Then, the VCO 67
outputs the sampling clock variably controlled on the
basis of the frequency control signal from the VCO
control unit 66.

15 This frequency control is carried out an and
after the third frame similarly thereto, whereby the
sampling clock with which the received OFDM signal is
sampled can be synchronized with the clock on the
transmission side at all times.

20 In addition, after the frequency control for
the reception sampling clock has been roughly stabi-
lized as in a fourth frame of Fig. 8, in the case where
the value of the reception sampling error information
ERR falls within a predetermined range (within ± 1 for
25 example) in such a way that a slight error of the
reception sampling clock frequency does not reflect the
count value of the frame counter 68, the correction for
the count value is not carried out at all. This reason

is that since the control for the reception sampling clock frequency is carried out in samples, the error of the reception sampling clock frequency can not be controlled within ± 1 clock in one frame.

5 By executing the above-mentioned processing, since the reception sample value sequence is synchronized with the count value of the frame counter 68, it is possible to be accurately aware of a specific time point such as a transmission point of the frame or the
10 symbol on the reception sample value sequence.

Next, description will hereinbelow be given with respect to the processing of regenerating the reception sampling clock, and demodulation processing after the control for the frame timing and the symbol
15 timing has been established with reference to Fig. 6 and Figs. 9 to 11.

Fig. 9 is a diagram showing the relation between the FFT time window of the FFT arithmetic operation unit 69 and the symbol, Fig. 10 is a diagram
20 showing a relation between a principle wave and a reflected wave when the delay time of the reflected wave is shorter than the guard interval, and Fig. 11 is a diagram showing the relation between the principle wave and the reflected wave when the delay time of the
25 reflected wave is longer than the guard interval. In this connection, in Figs. 10 and 11, the height of the rectangle showing the principle wave for one symbol period and the height of the rectangle showing the

reflected wave for one symbol period represent schematically the relation between the reception intensity of the principle wave and that of the reflected wave. That is, in each of Figs. 10 and 11, since the height of the rectangle of the principle wave is higher than that of the rectangle of the reflected wave, it is shown that the reception intensity of the principle wave is larger than that of the reflected wave.

10 In Fig. 6, first, the reception sample value sequence signal from the A/D conversion unit 62 is inputted to an FFT (Fast Fourier Transform) arithmetic operation unit 69.

Since the timing when the reception sample value sequence signal is inputted to the FFT arithmetic operation unit 69, i.e., the time window of the FFT utilizes generally the guard interval effectively, as shown in Fig. 9, it is the timing when the reception sample value sequence of the backward period of time (the effective data symbol unit) of the symbol is inputted, i.e., the time window thereof.

Now, since the OFDM modulated signal has the guard interval, as shown in Fig. 10, even if the reflected wave generated due to the presence of a mountain or building is inputted, the longitudinal symbol is not mixed therewith at all as long as the delay time falls within the guard interval period of time.

wave.

Fig. 24 is a diagram showing that, in order to obtain a less inter-symbol interference, the FET time window should be synchronized with which one of the principle wave or a reflected wave when the reflected wave has a longer delay time than the guard interval length.

Now, the axis of ordinate shown in Fig. 24 represents the D (Desired)/U (Undesired) ratio of the level of the principle wave to the level of the reflected wave in decibels, and the axis of abscissa represents the delay time of the reflected wave. In this connection, in this case, it is assumed that the effective symbol length of the OFDM data symbol is 51.2 μ sec, and the guard interval length is 1.6 μ sec.

In this figure, it is shown that in the area (white part) of the upper part of the graph, the inter-symbol interference becomes less when the FFT time window is provided in the timing of the principle wave, while in the area (oblique line part) of the lower part of the graph, the inter-symbol interference becomes less when the FFT time window is provided in the timing of the reflected wave. In addition, in the case where a level of the principle wave is higher than that of the reflected wave when the delay time is within the guard interval, as described above, the time window of the FFT is always provided in timing with the principle wave, whereby the inter-symbol interference is not

caused at all.

Thus, when a reflected wave is present with the delay time longer than the guard interval length, the FET time window should be provided in timing with which one of the principal wave or the reflected wave for a less inter-symbol interference depends on the delay time and the level of the reflected wave.

Now, taking the operation in the mobile transmission into consideration, as described above, since the state of the transmission path is changing every moment, the cross-correlation value sequence is changed as shown in the examples of Figs. 12 and 13. For example, the correlation peak brought by the principle wave becomes large in a certain frame, while the correlation peak brought by the reflected wave becomes large in the next frame, and so forth. Thus, the fluctuation of the correlation peak values of the principle wave and the reflected wave in the cross-correlation value sequence becomes violent.

As described above, since the correlation maximum value position detection unit 65 follows such a fluctuation of the cross-correlation value sequence, the position of the time window when detecting the maximum value changes depending on the state of the transmission path, and the value of the error information ERR will also change.

This is reflected to the VCO control unit 66, and as a result, the reception sampling clock frequency

outputted from the VCO 67 is also changed so that the proper demodulation processing can not be carried out in the demodulation processing unit 6A.

In addition, since the fluctuation of the error information ERR brings the fluctuation of the count value of the frame counter 68, there arises a problem that both of the frame timing and the symbol timing also fluctuate.

In the light of the foregoing, the present invention is intended to solve the above-mentioned problems, and it is therefore an object of the present invention to provide an OFDM digital transmission method in which the inter-symbol interference is less and hence the C/N ratio is better and an apparatus employing the same, and a method and an apparatus for receiving an OFDM signal.

It is another object of the present invention to provide an OFDM digital transmission method by which the processing of synchronizing a reception sampling clock, and the control for the frame timing and the symbol timing can be suitably carried out, and an apparatus employing the same, and a method and an apparatus for receiving an OFDM signal.

It is still another object of the present invention to provide an OFDM digital transmission method by which even when a cross-correlation peak value fluctuates in the operation of a mobile transmission apparatus or the like which undergoes the

signal is generated in accordance with which the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are carried out.

5 According to another feature of the present invention, if the above-mentioned effective correlation peak can not be detected, then the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are
10 suspended to hold the control state right before the suspension.

 According to a further feature of the present invention, the control is carried out on the basis of the above-mentioned effective correlation peak in such
15 a way that the reception sampling clock frequency is synchronized with the sampling clock on the transmission side.

 More specifically, a receiver according to the present invention may operate such that an
20 arithmetic operation of the cross-correlation between the received signal and a predetermined synchronous symbol is carried out to acquire a cross-correlation value sequence signal; and out of the cross-correlation value sequence signal thus acquired, a plurality of
25 correlation peaks are detected which are derived by the principle wave or the reflected wave. Each of the magnitudes of the detected correlation peak values is compared with the magnitude of a predetermined value.

contained in a cross-correlation value sequence signal
acquired from the arithmetic operation of the correla-
tion, detecting an effective correlation peak brought
by the principle wave, and on the basis of the effec-
5 tive correlation peak thus detected, carrying out the
the reception sampling clock synchronous processing and
the control for the frame timing and the symbol timing
of the receiver.

In the operation of the OFDM data trans-
10 mission in which the reflected wave having a delay time
longer than the guard interval and having a high level
can substantially be assumed to be absent, there exist
no such reflected wave which when synchronization is
made therewith, would provide a less inter-symbol
15 interference. Therefore, by setting the FFT time
window on the basis of the correlation peak brought by
the principle wave, the inter-symbol interference can
be either removed or substantially disregarded.

In this connection, as for technologies
20 associated with the OFDM transmission, reference may be
made to U.S. Serial No. 09/096454, Seiichi Sano et al.
filed on June 11, 1998 entitled "DATA TRANSMISSION
APPARATUS AND RECEIVING APPARATUS USING ORTHOGONAL
FREQUENCY DIVISION MULTIPLEX MODULATION SYSTEM" and
25 U.S. Serial No. 09/203564, Seiichi Sano et al. filed on
December 2, 1998 entitled "SYNCHRONIZATION DETECTION
METHOD FOR DATA TRANSMISSION APPARATUS AND DATA
TRANSMISSION APPARATUS USING THE SAME". The disclo-

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asures of these prior applications are hereby incorporated by reference herein.

BRIEF DESCRIPTION OF THE DRAWINGS.

The foregoing and other objects and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention as illustrated in the accompanying drawings wherein:

Fig. 1 is a block diagram showing a configuration of an embodiment of a receiver according to the present invention;

Fig. 2 is a wave form chart useful in explaining one example of an OFDM modulated signal;

Fig. 3 is a wave form chart useful in explaining one example of an OFDM symbol;

Fig. 4 is a wave form chart useful in explaining the structure of a transmission frame of the OFDM modulated signal;

Fig. 5 is a block diagram showing a configuration of a transmitter of one example in an OFDM transmission apparatus;

Fig. 6 is a block diagram showing a configuration of a receiver of one example in the OFDM transmission apparatus;

Fig. 7 is a graphical representation showing one example of the state of a cross-correlation value sequence signal;

the synchronization is made.

DESCRIPTION OF THE EMBODIMENTS

A digital transmission according to an embodiment of the present invention will hereinafter be described in detail with reference to the accompanying drawings. In this connection, in the figures, the same parts are designated with the same reference numerals.

Fig. 1 is a block diagram showing a configuration of a receiver of a digital transmission apparatus according to one embodiment of the present invention.

In Fig. 1, a received signal transmitted from a transmitter like one shown in Fig. 5 to reach the receiver through a transmission path is first converted from a signal having a inter frequency (IF) band to a signal having a base band frequency band in an IF/BB conversion unit 61, as described with reference to Fig. 6.

An output signal from the IF/BB conversion unit 61 is subjected to the analog/digital conversion in an A/D conversion unit 62 using a reception sampling clock. A reception sample value sequence signal acquired from the A/D conversion unit 62 is inputted to a null symbol detection unit 63, a sweep symbol correlation arithmetic operation unit 64 and an FFT arithmetic operation unit 69. The null symbol detection unit 63 detects a null symbol from the reception

sample value sequence signal to detect roughly a starting point of a frame. An output signal NS from the null symbol detection unit 63 is inputted to the sweep symbol correlation arithmetic operation unit 64 and then the arithmetic operation of the cross-correlation between the reception sample value sequence signal and a sweep symbol which is previously set is carried out in timing with the frame starting signal NS to acquire a cross-correlation value sequence.

10 Description will hereinbelow be given with respect to the operation of the receiver including an effective correlation position detection unit 1 according to the present invention.

Fig. 15 is a block diagram showing a configuration of the effective correlation position detection unit 1. The effective correlation position detection unit 1 is constituted by an effective correlation peak detection unit 11 and a control state protection unit 12. In addition, the detailed configuration of the effective correlation peak detection unit 11 is shown in Fig. 16.

A cross-correlation value sequence signal as an output signal from the sweep symbol correlation arithmetic operation unit 64 is inputted to a DFF (a D-type flip-flop) 114 an output signal of which is in turn inputted to a DFF 115. Now, if the cross-correlation value sequence signal as shown in Figs. 7, 12 and 13, and the like, as shown in Fig. 17, is

and $C(T) - C(T - 1) < 0$ (a differential coefficient has a tendency to be decreased) ... (2)

it can be said that the peak is present in the cross-correlation value sequence signal, and also the peak
5 value at this time is $C(T - 1)$.

Describing the above-mentioned expression (1) on the basis of the configuration of the effective correlation peak detection unit 11, $C(T - 2)$ as the output signal from the DFF 115 is subtracted from $C(T -$
10 1) as the output signal from the DFF 114 in a subtracter 117.

The subtracter 117 carries out the subtraction of $C(T - 1) - C(T - 2)$ to output the most significant code bit of the subtraction result in order
15 to show whether the result of the arithmetic operation is a positive number or a negative number. When the subtraction is carried out using the 2s complement, if the code bit is 0, then it is shown that the subtraction result is a positive number, while if the code bit
20 is 1, then it is shown that the subtraction result is a negative number.

In addition, likewise, describing the above-mentioned expression (2) on the basis of the configuration of the effective correlation peak detection unit
25 11, $C(T - 1)$ as the output signal from the DFF 114 is subtracted from $C(T)$ as the input signal to the DFF 114 in a subtracter 116. This subtracter 116 carries out the subtraction of $C(T) - C(T - 1)$ to output similarly

is small, a large number of correlation peaks are present. Those correlation peaks each having a low level are not the correlation peaks each of which is generated when the time window of the arithmetic
5 operation of the cross-correlation coincides with the sweep symbol of the principle wave or the reflected wave, but are generated due to the noises.

Therefore, in order to remove any of the correlation peaks due to the noises, as shown in Fig.
10 18, a predetermined value is set in the cross-correlation value sequence and then the correlation peak is judged to be the effective correlation peak when the value of the correlation peak is equal to or larger than the predetermined value. In such a way, a
15 plurality of effective correlation peaks brought by the principle wave or the reflected wave are detected from within the acquired cross-correlation value sequence.

Describing this operation, this predetermined value is outputted from a threshold generator 111. The
20 predetermined value is either previously set to a fixed value or set to an arbitrary fraction of the level of the reception sample value sequence to make follow the level of the reception sample value sequence.

The output signal from the threshold
25 generator 111 is inputted to a minus input terminal of a comparator 112. In addition, to a plus input terminal of the comparator 112 is inputted $C(T - 1)$ as the value of the correlation peak, i.e., an output

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reflected wave is present the delay time of which exceeds the guard interval, it can be discriminated from Fig. 24 that it may be better to provide the FET time window in synchronism with which one of the
5 principle wave or the reflected wave on the basis of the D/N ratio.

Next, the operation of the interference discrimination unit 11C will hereinbelow be described in detail.

10 The interference discrimination unit 11C judges that when the logical value at the PK terminal becomes 1 as described above, each of the correlation peak values at the DATA terminal and each of the sample number at the LOC terminal are valid, and stores those
15 values in memory means such as a RAM (Random Access Memory) or an FF (Flip-Flop)(not shown). In other words, for example, in the case as shown in Fig. 18, the two effective correlation peak values brought by the principle wave and the reflected wave, respec-
20 tively, and the corresponding sample numbers are all stored therein.

Then, the level difference (the D/U ratio) between the principle wave and the reflected wave is arithmetically operated on the basis of those effective
25 correlation peak values. As for the method of operating arithmetically the D/N ratio, the division between the level of the principle wave and the level of the reflected wave is carried out, and the logarithmically

arithmetic operation is carried out for the division result, whereby it is possible to operate arithmetically the D/U ratio. In addition, the sample number of the principle wave is subtracted from the sample number of the reflected wave to operate arithmetically the delay time in sampling clocks.

Thus, by using the relation between the arithmetically operated D/U ratio and the delay time shown in Fig. 24, it is judged that, in order to obtain a less inter-symbol interference the FET time window should be in synchronism with which one of the correlation peak of the principle wave or that of the reflected wave, and then on the basis of the judgement result, the correlation peak in which the inter-symbol interference is least is made the correlation peak for establishment of synchronization.

However, the arithmetic operation circuit for carrying out the arithmetic operation for the correlation peak values brought by the principle wave and the reflected wave, and the delay time to discriminate the condition shown in Fig. 24 requires a very large circuit scale. For this reason, the method is easier wherein it is previously arithmetically operated that does the inter-symbol interference become less when with which of the principle wave or the reflected wave the synchronization is made in correspondence to the correlation peak values brought by the principle wave and the reflected wave, and the delay time, and this

sampling clock frequency, and the fluctuation of the frame timing and the symbol timing may occur in some cases.

When the state of the transmission path is stable, the stable reception sampling clock is supplied to the receiver, both of the frame timing and the symbol timing are also stable, and the principle wave having a high level stably reach the receiver, the control state protection unit 12 operates in such a way that the effective correlation peak brought by the principle wave is made the correlation peak for establishment of synchronization in the receiver, and on the basis of this effective correlation peak, the control for the reception sampling clock frequency, and the control for the frame timing and the symbol timing are carried out.

On the other hand, when the state of the transmission path is of very poor quality and hence the stable principle wave does not reach the receiver, the control state protection unit 12 has the function of suspending the above-mentioned control in the receiver and carrying out the demodulation while maintaining the state experienced when the principle wave stably reaches the receiver.

This operation of the control state protection unit 12 will hereinbelow be described in detail with reference to a timing chart shown in Fig. 21.

When the synchronization is unestablished,

the error information MERR outputted from the effective correlation peak detection unit 11 fluctuates largely, and hence the control for the reception sampling clock frequency and the control for the frame timing and the symbol timing are carried out.

Thereafter, when the synchronization is established and the state of the transmission path also becomes stable, the fluctuation of the error information MERR becomes less (e.g., the fluctuation amount falls within ± 1).

A comparator 121, when the inputted error information MERR falls within a predetermined range (e.g., ± 1), exhibits the stable reception state to output the logical value of 1.

However, when the state of the transmission path which has been stable till now fluctuates to bring the cross-correlation value sequence as shown in Fig. 20, and the correlation peak value of the principle wave in the comparator 112 shown in Fig. 16 becomes smaller than a level of the threshold generator 111, the fluctuation of the error information MERR becomes abruptly large, and also the value of the error information MERR exceeds a predetermined range (e.g., ± 1). At this time, the comparator 121 exhibits that the state of the transmission path fluctuates and becomes unstable to output the logical value of 0.

In addition, PKF as the flag exhibiting that the effective correlation peak is present is inputted

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to one input terminal of an AND circuit 122. An output signal from the comparator 121 is inputted to the other input terminal of the AND circuit 122. When the two conditions are established that PKF is 1, i.e., the effective correlation peak is present, and the logical value of the output signal of the comparator 121 is 1, i.e., the state of the transmission path is stable, the AND circuit 122 outputs the logical value of 1.

An output signal from the AND circuit 122 is inputted to a U/D terminal of the updown counter 124. The updown counter 124 up-counts the count value when the logical value of the signal at the U/D terminal is 1, while down-counts the count value when the logical value of the signal at the U/D terminal is 0.

After the updown counter 124 counts the count value up to the value outputted from a counter upper limit value generator 123 (in Fig. 21, an output value thereof is set to 10 for example), it holds the count value for a period of time ranging from that time point (t1) to a time point when the logical value of 0 is inputted to the U/D terminal.

In such a manner, the fact that the count value is held at the value in the counter upper limit value generator 123 means that the state of the transmission path is within a period of time from t1 to t2 when it is regularly stable.

An output signal from the updown counter 124 is inputted to one input terminal of a comparator 126,

Therefore, since for a stable period of time from t_0 to t_2 , the logical value of the output signal from the AND circuit 122 is 1, the logic of the input signal to the AND circuit 129 is inverted in the inverter 128 to be 0, and hence the logical values of the two input signals to the AND circuit 129 become 1 and 0, respectively, so that the logical value of the output signal from the AND circuit 129 becomes 0.

An output terminal of the AND circuit 129 is electrically connected to a switching terminal of a selector 12A. Then, the selector 12A, when the logical value of the signal at the switching terminal is 0, outputs a signal at an I0 terminal as the error information signal ERR and when the logical value of the signal at the switching terminal is 1, outputs a signal at an I1 terminal.

Therefore, since for a period of time from t_0 to t_2 , the logical value of the input signal at the switching terminal is 0, the selector 12A outputs as it is the signal at the I0 terminal, i.e., the error signal MERR as the error information ERR to apply the error information ERR to the VCO control unit 66 to control the VCO 67 in such a way that the reception sampling clock frequency is synchronized with the sampling clock frequency on the transmission side.

However, when the state of the transmission path fluctuates from the regularly stable state to the unstable state in an instant (for a period of time from

t2 to t3), the logical value of the output signal from the AND circuit 122 exhibiting the state of the transmission path becomes 0, and hence the updown counter 124 starts to carry out the down-count. However, in this case, since the count value of the updown counter 124 is larger than the value of the protection value generator 125, the comparator 126 outputs the logical value of 1.

Then, in this case, since the logical value of the output signal from the AND circuit 122 becomes 0 to be inverted in the inverter 128, the logical value of the input signal to the other input terminal of the AND circuit 129 becomes 1, and hence the AND circuit 129 outputs the logical value of 1.

As a result, on the basis of the output signal having the logical value of 1 from the AND circuit 129, the terminal of the selector 12A is switched over to the I1 terminal side so that the selector 12A outputs as the error information signal ERR an output signal having the logical value of 0 from a zero-value generator 127 in accordance with which the logical value of the error information signal ERR which is used to control the VCO 67 is made 0.

At the time when the logical value of the error information ERR becomes 0, the VCO control unit 66, on the assumption that the reception sampling clock frequency error is absent, holds the frequency-controlled voltage of the VCO 67 at the current value.

In such a manner, when the situation of the transmission path fluctuates in an instant from the regularly stable state to the unstable state, the demodulation operation is carried out while holding the control state exhibited when the reception has been stably carried out.

Then, for a period of time from t_3 to t_4 when the state of the transmission path is stable, the same processing as that for a period of time from t_0 to t_2 is executed to output as the error information the signal MERR as it is.

Next, description will hereinbelow be given with respect to the case where the state of the transmission path becomes continuously unstable as for a period of time from t_4 to t_6 .

First, for a period of time from t_4 to t_5 when the output value from the updown counter 124 is larger than the value of the protection value generator 125 and hence the comparator 126 outputs the logical value of 1, the same processing as that for a period of time from t_2 to t_3 is executed, and the logical value of the error information signal ERR is made 0 to hold the current control state.

However, at the time when the magnitude of the output signal from the updown counter 124 becomes smaller than the value of the protection value generator 125 (at a time t_5), the logical value of the output signal from the comparator 126 becomes 0, and

reference symbol and the received signal sequence is carried out, whereby similarly to the sweep symbol, the control for the FFT time window position and the control for the VCO frequency can also be carried out.

5 As set forth hereinabove, in the receiver according to the above-mentioned embodiment, even in the case where the state of the transmission path is of very poor quality and hence the composite signal of the principle wave and the reflected wave is received as
10 the received signal, and also the level of the reflected wave becomes larger than that of the principle wave, the control for the frame timing and the symbol timing, i.e., the control for the time window of the FFT arithmetic operation is carried out
15 in such a way that the inter-symbol interference becomes minimum, whereby it is possible to suppress the degradation of the code error rate.

 In addition, in the case where the state of the transmission path fluctuates in the operation of
20 the mobile transmission or the like and hence the correlation peak value in the receiver fluctuates, when the state of the transmission path is of very poor quality, and hence the stable principle wave does not yet reach the receiver, the control for the reception
25 sampling clock frequency is suspended to hold the state obtained when the stable reception is carried out, whereby it is possible to continue to supply stably the reception sampling clock.

